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Design of engineered elastomeric substrate for stretchable active devices and sensors

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Abstract

In the field of flexible electronics, emerging applications require biocompatible and unobtrusive devices, which can withstand different modes of mechanical deformation and achieve low complexity in the fabrication process. Here, the fabrication of a mesa-shaped elastomeric substrate, supporting Thin-Film Transistors (TFTs) and logic circuits (inverters), is reported. High-relief structures are designed to minimize the strain experienced by the electronics, which are fabricated directly on the pillars' surface. In this design configuration, devices based on amorphous Indium-Gallium-Zinc-Oxide can withstand different modes of deformation. Bending, stretching and twisting experiments up to 6 mm radius, 20 % uniaxial strain and 180° global twisting, respectively, are performed to show stable electrical

performance of the TFTs. Similarly, a fully integrated digital inverter is tested while stretched up to 20 % elongation. As a proof of the versatility of our mesa-shaped geometry, a biocompatible and stretchable sensor for temperature mapping is also realized. Using Pectin, which is a temperature-sensitive material present in plant cells, the response of the sensor shows current modulation from 13 °C to 28 °C and functionality up to 15 % strain. These results demonstrate the performance of highly flexible electronics for a broad variety of applications, including smart skin and health monitoring.

The request for highly stretchable (strain > 10 %) and conformable electronics, capable to yield high performance, as well as to resist different modes of deformation, is continuously increasing.^[1,2] Interesting applications for this technology include smart textiles,^[3,4] emerging electronic devices, such as curvy and rollable displays,^[5,6] and bio-integrated systems.^[7,8] Most of the recent research in this area has focused on the discovery of suitable materials for these applications^[9,10] (such as organic semiconductors, polymeric dielectrics,...). In parallel, the development of novel approaches to minimize the stresses experienced by devices on flexible substrates, have demonstrated the ability to increase stretchability also for conventional electronic materials. For example, the transfer of either ultra-thin membranes (< 1 µm) or brittle electronics on composite substrates has been shown.^[11,12] Also, the encapsulation of stiff islands (10-90 µm thick SU8 epoxy resist)^[13] or fluids (ionic [EMIM][EtSO₄] solution or silicone oligomer)^[14,15] in the flexible substrates has allowed to isolate the strains in areas surrounding the electronic components. In this way, Thin-Film Transistors (TFTs), temperature sensors as well as mechano-acoustic sensors have been presented,^[14,15] with the drawback of a more complex fabrication process. Finally, buckled electronics, generally realized by inducing wrinkles^[16,17] or by releasing the initial strain

applied on the substrate, have been demonstrated to realize polymeric light emitting diodes (PLEDs)^[18] and magnetic sensors.^[19]

Here, we present a technique to fabricate a highly flexible substrate shaped with mesa (or pillar) structures that support the electronic devices. During mechanical solicitations, the use of such high-relief structures aims at localizing the strains on the substrate, around the pillars and not on the pillars' surface. We perform a numerical parametric study, to engineer the appropriate geometrical features, and then, we fabricate the engineered substrate using PDMS (Polydimethylsiloxane). Experiments, using thin-film resistors as reference structures, validate the Finite Element Analysis (FEA) and demonstrate an improvement of the substrate stretchability by twelve-fold with respect to a flat, standard geometry. Next, Thin-Film Transistors (TFTs) and logic circuits (inverters), based on amorphous Indium-Gallium-Zinc-Oxide (a-IGZO), are directly fabricated on the pillars, using shadow masking and UV photolithographic processes. The devices are electrically characterized under different modes of deformations and show no performance degradation while bent to a radius of curvature equal to 6 mm, stretched to 20 % and twisted to 180°. To prove the versatility of our approach, a biocompatible and flexible temperature sensor is realized through the combination of our engineered substrate and Pectin, which is a temperature-sensitive material present in plant cells.^[20] The resistive response of the sensor allows the temperature monitoring in a range from 13°C to 28 °C, with a reported sensitivity equal to 10 mK.^[20] We demonstrate the functionality of the temperature sensor in flat and stretched (up to 15 %) condition.

The basic design of the engineered substrate is characterized by raised regions (called "pillars" or "mesa", **Figure 1a**), with variable geometrical parameters. By design, the mechanical strain experienced by the pillars, is lower than the one applied on the entire substrate for most modes of deformation. Differently from the “rigid island” approach^[13,21], where stiff patches are realized on/embedded in a stretchable matrix, here, the goal is to use a

molding process to fabricate an engineered substrate (using only one material) with high-pillar structures, where electronics can experience reduced strain (see Figure S1). A comparison with other implemented technologies is reported in Table S1. To enhance the flexibility of the overall system, it is crucial to understand how to minimize the strain on the surface of the pillars. First, the geometrical sizes of the pillars (width, height and pillar-to-pillar distance) are simulated (see Figure S2). For large substrate thickness (parameter 'h' > 500 μm , in Figure 1a), the strain on the pillar, ϵ_{pillar} , is minimized (see Figure S2b). At the same time, thick pillars (parameter 't' > 250 μm , in Figure 1a) allow a further increase of the applied strain $\epsilon_{\text{applied}}$, keeping unchanged ϵ_{pillar} (see Figure S2c). For this reason, a ratio of 70% between the substrate thickness and the pillar one (h/t, see Figure 1a) is chosen. When simulating the effects of variable spacing between two neighboring pillars (parameter 's' in Figure 1a, varied from 1 to 3 mm), no substantial differences in the strain evolution are denoted (see Figure S2d) ($\eta = \epsilon_{\text{pillar}} / \epsilon_{\text{applied}} < 5\%$). Considering that the electronics are fabricated only on the pillars' surface, the spacing distance between two neighboring pillars is made to have a high density of devices which can be realized on a single substrate. Taking into account all constraints, the PDMS membrane is designed to have a total thickness of 800 μm , a mesa thickness and edge of 560 μm and 5 mm respectively, a pillar-to-pillar spacing of 2.5 mm, and consequently a 9 x 9 pillars' array (see Figure 1a).

Another important point to improve the flexibility of our engineered substrate is the shape of the relief structures. For this analysis, 3D simulations are performed to understand whether the strain experienced on top of the pillars can be minimized. For this purpose, three shapes are studied: squared, hexagonal and circular, while keeping the pillar area constant. The FE sample is a squared membrane, with 17.5 mm side, consisting of four pillars (arranged in a 2 x 2 matrix). When a bi-axial strain (x-y plane direction) is applied on two perpendicular sides of the membrane (one in x-direction, and the other one in y-direction), the opposite ones have degree of freedom (DOF) equal to zero (namely, they cannot move or rotate). Under these

conditions, the circular mesa responds with an improved accommodation of the strain (Figure 1b, 1c and 1d). For an overall strain of 20% applied, the circular pillars are characterized by a 2% strain, ϵ_{pillar} , and a pillar-to-pillar elongation (parameter 's' in Figure 1a) of 110 %. For the same parameters, the square pillar reaches a local strain of 5 % and 165 % pillar elongation, while the hexagonal one, 3.6 % and 140 %. Digital Image Correction (DIC) method is used to map the strain distribution on the three different shapes by performing tensile measurements from 0 % to 40 % strain (acquisition frame rate 2S/s) (Figure 1e, 1f and 1g).

A key advantage of our engineered substrate consists in the possibility of reducing the strain distribution on the pillars' surfaces according to the target application. Indeed, by modulating the geometrical parameters of our mesa structures (width, height and pillar-to-pillar distance), the strain experienced on the pillars' surfaces can be lowered (see Figure S3).

For most applications, it is important to characterize the strain map of the engineered substrate when subjected to different types of mechanical deformations. For this, a model, in which a PDMS membrane is subjected to bending and twisting deformations, is presented in Figure 1h and 1i. To make the simulations more realistic, the elastomeric substrate is modeled with a 4 μm -thick polyimide foil and a 50 nm-thick Al_2O_3 layer, representing a planarization layer (used to smoothen the pillars' surface, see *Device fabrication* section) and the dielectric layer in the electronic device stack (see *Device fabrication* section).

For both bending and twisting simulations, the maximum principal strain is evaluated using a PDMS stripe, constituted by five pillars in line. In the bending study, the FE sample is clamped on both ends, one capable to move in one direction (DOF in y- and z-direction equal to zero, while DOF in x-direction different from zero, if motion occurs in x-direction), while the other one is fixed (DOF in all directions equal to zero). Here, the maximum principal strain on the pillar's surface is as low as 1 %. For the twisting analysis, the simulation is performed by clamping the sample on one side and twisting the other one. On the fixed clamp, all continuous nodes are constrained in the three dimensions; on the other clamp, all nodes are

mapped as a rigid body to one single reference point, where a rotation is applied. For a twisted angle of 180° , a maximum principal strain of 2.1 % is calculated. As expected, in this last type of deformation, the strain distribution ϵ_{pillar} is characterized by a symmetric behavior in the middle pillars (see Figure S4).

To validate our simulations with experiments, we first implement our engineered membrane on a glass substrate, used as mechanical support (see Figure S5 and *Substrate preparation* section). The sample consists of a squared PDMS membrane of 7.5 cm x 7.5 cm with a 9 x 9 array of pillars. We deposit thin-film resistors (hereafter, called also resistors) on top of the pillars, to monitor the strain on the pillar's surface. We analyze the surface of the elastomeric substrate by optical inspection of the devices and of the trench, while uniaxial stretching is applied on the membrane (see Figure S6). The surface strains measured experimentally agree with the FEA results (see Figure S6). We also evaluate the variation of the electrical resistance as a function of the applied strain on different pillars shape, under biaxial stretching (see Figure S7). The resistors preserve functionality up to a strain of 38 % in the case of circular pillars, with resistance variations below the other two selected shapes (see Figure S7e) (± 1.8 , for square pillars, ± 0.56 , for hexagonal ones, ± 0.08 , for circular ones). We also tested the response of resistors fabricated with different metals, with a more stable functionality displayed by Ti/Au layer (rather than Ti, Cr/Au and Cu) (see Figure S8). Based on the range of parameters analyzed, the overall stretchability of our electronics (fabricated on the pillars' surface) can be improved by twelve-fold with respect to a flat, standard geometry (see Figure S8).

Different electronic devices, like TFTs and inverters, are fabricated on the high-relief structures of our engineered substrate and afterward characterized while mechanical strain is applied. For these tests, all the devices are realized on 560 μm -thick round pillars with shadow masking and UV photolithographic processes. After the fabrication is complete, the

PDMS membrane is detached from the glass support and the devices performance is measured. The TFTs and inverters (NOT gates) are based on bottom-gate inverted staggered configuration (see **Figure 2a** and *Device fabrication* section). IGZO^[22-24] is chosen as semiconductor for its high electrical performance, low deposition temperature and large area capability, representing a good candidate as semiconductive material on flexible substrates.^[25,26] The transfer and output characteristics of an IGZO-based TFT directly fabricated on a mesa-shaped PDMS membrane are shown in Figure 2b and 2c. The TFT is characterized by a threshold voltage V_{TH} and subthreshold swing equal to 2.8 V and 0.23 V/dec, respectively. The threshold voltage is higher than on polyimide or PET,^[27,28] due to the unpassivation of the device, which generally improves the TFT performances thanks to the intrinsic annealing of the semiconductor (e.g. Al_2O_3 deposited at temperatures between 100°C and 200°C^[11]). The I_{ON}/I_{OFF} ratio is above 10^6 and allows digital circuit applications.^[23] The effective mobility μ_{eff} is equal to 1.2 cm²/Vs. Although the implemented planarization layer (see *Device fabrication* section), this low value can be attributed to a high surface roughness (as presented elsewhere^[29]). With appropriate smoothing layers (i.e. curing temperature < 150 °C), the pillar surface roughness can be optimized with an improvement of the TFT performances.

The device performances are then characterized under bending deformations. In this case, two types of experiments are performed: a static bending test, where the device is characterized while wrapped around a metallic rod using a double sided tape (3M 300 LSE, Young's modulus and thickness, $E_{tape} = 10$ MPa and $t_{tape} = 120$ μm, respectively) (see **Figure 3a** and Figure S9); a cyclic bending test, where the TFT functionality is tested, while the substrate is consecutively bent using a custom-made setup (see^[28] and Figure S10). For the static experiment, multiple bending radii down to 6 mm are tested, while, for the cyclic test, the TFT is bent up to 1000 times to 6 mm bending radius. The TFTs ($W/L = 224$ μm/ 8 μm) are electrically characterized and their transfer characteristics are displayed in Figure 3d and 3g.

Apart from the I_{ON}/I_{OFF} ratio which shows a value always above 10^6 , the other TFT parameters (threshold voltage shift ΔV_{th} , normalized Subthreshold Swing SS and normalized saturation mobility μ) have a maximum variation below 10 %, which is coherent with other works^[30] (see Figure S9). For these experiments, measurements below 6 mm are not possible due to the poor conformability of the PDMS membrane to any curved surface.

The performances of the electronic devices are also characterized in response to tensile deformations, for both static and cyclic solicitations. In the first case, the PDMS support is mounted on a biaxial custom made setup (see Figure S7), whereas, the system in Figure S10 is used for the dynamic experiments. As expected from the simulation results, the applied uniaxial stretching causes the pillars to deform (Figure 3b). The electrical characterization in Figure 3e and 3h displays the transfer characteristics of two different TFTs: one, statically stretched up to 20 % and reflattened, with an average change of the threshold voltage, Subthreshold Swing and normalized saturation mobility μ of 11.8 % (see Figure S10); another one, stretched for 1000 times to a maximum strain of 5 %, and showing a 5 % average variation of the parameters (see Figure S10). In both cases, the I_{ON}/I_{OFF} ratio shows stable trends over the stretching ranges (value always greater than 4.8×10^6 , for the static experiment, and greater than 2.9×10^7 , for the cyclic one).

Taking advantage of the design of our engineered substrate, the IGZO-based TFTs are evaluated under twisting condition. For these tests, a custom-made system, consisting of a fixed clamp and a moveable one, is assembled (Figure 3c). As demonstrated in Figure S4, the strain is equal in all the middle pillars (namely, the ones not clamped) and independent on their position on the membrane. In the static tests, the PDMS stripe is turned from 0° to an angle (from $+45^\circ$ to $+180^\circ$), back to 0° , and then electrically characterized; while, in the cyclic experiment, the membrane is repeatedly twisted from -90° to $+90^\circ$. In Figure 3f and 3i, the transfer characteristics are displayed, while output characteristics and parameter variations

are shown in Figure S11. A demonstration of the different mechanical tests is presented in the video S1.

To prove the scalability of our fabrication process, logic NOT gates are also realized (see Figure 2a). The inverter is based on a pseudo-NMOS configuration, where two TFTs are implemented: one, the driver TFT ($W/L = 280 \text{ } \mu\text{m}/ 10 \text{ } \mu\text{m}$), is connected in series with the second one, a load TFT ($W/L = 35 \text{ } \mu\text{m}/ 35 \text{ } \mu\text{m}$) (see **Figure 4a, 4b**). The device functionality is proved for uniaxial stretching up to 20 % and then reflattened (see Figure 4c). The mechanical strain is applied perpendicularly to the drain-source current direction. By monitoring its performance, the inverter exhibits maximum variation from the flat condition of 1.2 μs , for the propagation delays (constant trend, for the propagation delay from low to high $T_{PD \text{ L} \rightarrow \text{H}}$, 1.2 μs , for the propagation delay from high to low $T_{PD \text{ H} \rightarrow \text{L}}$), and 6.4 μs , for the falling/rising times (1.2 μs , for the falling time T_{FALL} , and 6.4 μs , for the rising time T_{RISE}) (see Figure S12). The propagation delays and falling/rising times are calculated considering an output load of 1 M Ω and 1 pF, due to the active probe used for the inverter characterization. Based on this performance, the maximum operation frequency for the inverter ($f_{\text{max}} = 1 / (T_{\text{RISE}} + T_{\text{FALL}})$) is 71 kHz.

In general, the reasons for the electronics (TFTs and inverters) failure are mainly correlated to the gate dielectric. Indeed, when the engineered substrate is released from the glass carrier (see Figure S5), cracks in the Al_2O_3 layer can occur, with consequent high gate leakage current measured during the device characterization (not shown here).

In the last years, a great focus in the field of flexible electronics was dedicated to LEDs systems which can accommodate different modes of deformation.^[18,31,32] Emerging applications such as pain relief techniques^[33] and wound healing approaches^[34] require optoelectronic systems capable to accommodate the applied strain. As an illustrative example, a 9 x 5 matrix is realized by mounting a commercial light-emitting diode (LED) on each pillar (see Figure S13a and *Device fabrication* section). The PDMS membrane is forced to undergo

bending and stretching conditions (see Figure S13b and c). The DC voltage inputs of 2 V and 3.3 V (for the red LEDs, and for the green and blue ones, respectively), are applied through standard Cu wires. Despite the applied mechanical strain, the device functionality remains unchanged (see video S2).

For the design of a complete stretchable system, the combination of active electronic devices and sensors is required. Together with strain^[35,36] and pressure^[37,38] sensors, temperature-sensitive devices, which can be stretchable and biocompatible at the same time, allow the implementation of non-invasive and unobtrusive systems for health monitoring. As proof of concept, our engineered elastomeric substrate is combined with a layer of Pectin, a plant-derived molecule recently reported to have large temperature-responsivity^[39,40] (see *Device fabrication* section). The temperature sensor, consisting of a single pillar (acting as substrate), metal contacts and the Pectin layer (see **Figure 5a**), is mounted on a heating/cooling system (see Figure S14). To highlight the sensor functionality (rather than the mechanical properties), hexagonal-shaped pillars are implemented. Although the Pectin guarantees functionality on a wide temperature range (from 0 °C to 45 °C), with sensitivity equal to 10 mK,^[20] the resistive response of the sensor (current modulation through the Pectin layer normalized with respect to the current at 23°C) is here monitored while the temperature is swept from 13°C to 28 °C (current at 13°C, $I_{13^{\circ}\text{C}} = 0.24 \mu\text{A}$, current at 28°C, $I_{28^{\circ}\text{C}} = 1.3 \mu\text{A}$) (see *Thermal characterization* section) (see Figure 5b). The upper temperature reached in this experiment (28 °C) is limited by the experimental setup used, and not by the Pectin (which has already been demonstrated to work up to 55 °C.^[20] Moreover, the mechanical properties of the sensor are evaluated by comparing its performance in flat condition and while stretched up to 15 % strain (see inset Figure 5b). The functionality of the sensor is proved by the acquisition of thermal images (see Figure 5c) at two different temperatures ($T_1 = 14^{\circ}\text{C}$ and $T_2 = 28^{\circ}\text{C}$), to resemble the “cold” and “warm” condition. Considering the substrate and Pectin

biocompatibility,^[41] this finding demonstrates the realization of a flexible and biocompatible temperature sensor, with potential applications in health monitoring or wearable devices.

The use of stretchable interconnections among the pillars^[42,43] can enhance the outcomes. At the same time, the implementation of conductive PDMS (i.e. using Silver nanowires^[44]) to form the engineered substrate, would allow the electrical connection between the electronics on the pillar surface with rigid boards (see Figure S15) and pillar-to-pillar interconnections. In this direction, different strategies and materials have been demonstrated in the fabrication of stretchable conductors, with stable functionality above 50 % strain.^[45] The implementation of soft and stretchable circuit boards can allow pioneering applications, especially in the field of biomedical devices.

The realization of an engineered mesa-shaped substrate for stretchable electronics is presented. The use of high-relief features, like pillars structures, allows mechanical decoupling of the overall strain (applied on the membrane) and the strain experienced by the electronic devices. This approach enables the realization of TFTs and circuits, capable of resisting different modes of deformations. In this way, the electronics, fabricated directly on the pillars, are functional while bent down to 6 mm bending radii, stretched up to 20 % and twisted up to 180°. By combining electronic components to a sensing layer, we demonstrate the ability to incorporate on the substrates also temperature sensors, which showed current modulation ranging from 13°C to 28°C under mechanical deformations. The design of the PDMS substrate together with the realization of different devices proves a promising technique for highly flexible and biocompatible electronics for smart textiles and implantable diagnostics.

Experimental Section

Substrate preparation: For the substrate preparation, an Aluminum mold, resembling the desired shape (squared, hexagonal and circular) and the simulated pillar geometrical sizes ($w = 5 \text{ mm}$, $s = 2.5 \text{ mm}$, $t = 560 \text{ }\mu\text{m}$ and $h = 800 \text{ }\mu\text{m}$), is used. First, a $800 \text{ }\mu\text{m}$ thick PDMS layer (Dow Corning Sylgard 184, mixed in a 10:1 weight ratio) is spin coated on the mold and cured at $150 \text{ }^{\circ}\text{C}$ for 10 minutes. Separately, a 3" x 3" glass support is coated by a $80 \text{ }\mu\text{m}$ thick PDMS layer (also in this case, the elastomer substrate is cured at $150 \text{ }^{\circ}\text{C}$ for 10 minutes). In order to bond the mold and the glass, first, a thin layer of PDMS curing agent is spin coated on the latter one; then, they are placed together and cured on hotplate at 150°C for 10 minutes. Finally, the Al mold is released by carefully using a cutter, leaving the mesa-shaped substrate on top of the glass (which will act as carrier support for the device fabrication). A schematic of the process is shown in Figure S5.

Device fabrication: The fabrication of the devices starts with a O_2 plasma treatment performed for 1 minute, to improve the adhesion between the PDMS and the device layers. The resistors are realized by deposition of thin metal layers (Ti 50 nm, Ti/Au 10/60 nm, Cr/Au 10/60 nm, Cu 50 nm) (see Figure S7 and S8) by e-beam evaporation and structured by shadow masking. The TFTs are implemented in a bottom-gate structured architecture. First, a $4 \text{ }\mu\text{m}$ polyimide layer (HD4100) is spin coated on the pillar as planarization layer, to smoothen the rough surface of the PDMS (due to the Al metallic mold). The gate contact is composed by a 10/60 nm-thick bi-layer of Ti/Au, deposited by shadow masking. As gate dielectric, a 50 nm-thick aluminum oxide (Al_2O_3) (dielectric constant: 9.5) layer is deposited by atomic layer deposition (ALD) at $150 \text{ }^{\circ}\text{C}$, which is the highest temperature encountered during the fabrication. Then, the amorphous-IGZO semiconductor is RF sputtered at room temperature, and, later, structured by wet etching in a diluted Hydrochloric acid ($\text{HCl} : \text{H}_2\text{O}$ 1:120) for 45 seconds. The contact vias are patterned and etched by a 50 ml H_2O + 45 ml CH_3COOH (acetic acid) + 10 ml HNO_3 (nitric acid) + 250 ml H_3PO_4 (phosphoric acid)

solution, heated to a temperature of 50 °C for 30 seconds. As source and drain contacts, a 100 nm layer of Cu is deposited by e-beam evaporation and structured by wet etching in Iron chloride solution (156 mg Iron chloride (FeCl_3) + 364 ml H_2O) for 20 seconds. For the TFTs layer structuring, standard UV lithography is used.

For the LED matrix, an engineered PDMS substrate with square pillars is used. A 10/100 nm thick Ti/Au layer is deposited as metal contact by e-beam evaporation and structured by shadow masking for the ground and supply voltage pads. Three colors LEDs are used: red (OSRAM LS R976), green (LTST-C170TGKT) and blue (LTST-C171TBKT). In order to ensure a good electrical contact between the LEDs and the evaporated metal, a conductive epoxy resin (EPO-TEK EJ2189) is used (cured at 100°C for 1 h), while standard Copper wires (50 μm in diameter) are used for interconnections between the pillars.

The temperature sensor consists of metal pads, formed by a Ti/Pt bilayer with a thickness of 10/60 nm deposited by evaporation, and a 5 μl Pectin layer deposited with the use of a pipette on the pillar surface. The Pectin is produced by the combination of commercially available citrus low-methoxylated pectin (LMP) with a methylation degree of 34 % and a galacturonic acid content of 84 % (Herbstreith&Fox[®]). Pectin powder is dissolved in deionized water at 80°C, and then deposited on each pillar by using a pipette. To jellyfy the temperature-sensitive layer, a 32 mM CaCl_2 solution is prepared and then added on the pillar surface. Finally, the whole substrate with the Pectin layer is transferred to a vacuum chamber and dehydrated at 12 mbar overnight.

Electrical Characterization: The TFTs are characterized by using an Agilent B1500A parameter analyzer under ambient conditions. The bending experiments are described in^[46] and,^[28] while for the stretching and twisting ones, two custom-made setups are implemented (see Figure S7 and 3c). For the circuit measurement, a HP 6626A power supply, an Agilent MSO-X-3014A oscilloscope and an Agilent 33522A waveform generator are used. For the LEDs matrix, a HP E3631A DC Power Supply is used.

Thermal Characterization: The temperature on the Pectin film is activated by a Peltier-Element MS3 (Laird Technologies) and acquired by a IR thermal camera (FLIR A655sc). To control the temperature on the Peltier, a custom made PI controller with a power output stage is utilized (see Figure S14). A source meter (Keithley model 2635) and standard probe needles are used to monitor the current modulation of the Pectin layer through the Ti/Pt metal pads.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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G. C. and V. C. contributed equally to this work. G.C. conceived the work and wrote the manuscript. V. C. realized and measured the temperature sensor. V.C and L.B performed the DIC measurements. A. F. implemented the substrate and fabricated the active devices. R. H. simulated the mechanics of the system. A. C., G.C, C.V., M. V., L.P., N.M., L.B., G.A.S., A.D., S.K., carried out the experiments and characterization. C. D. and G.T. supervised the work and contributed to the writing of the manuscript. This study was supported by the ETH grant n.0-20949-13 and in part by the Samsung Advanced Institute of Technology (SAIT)'s Global Research Outreach (GRO) Program.

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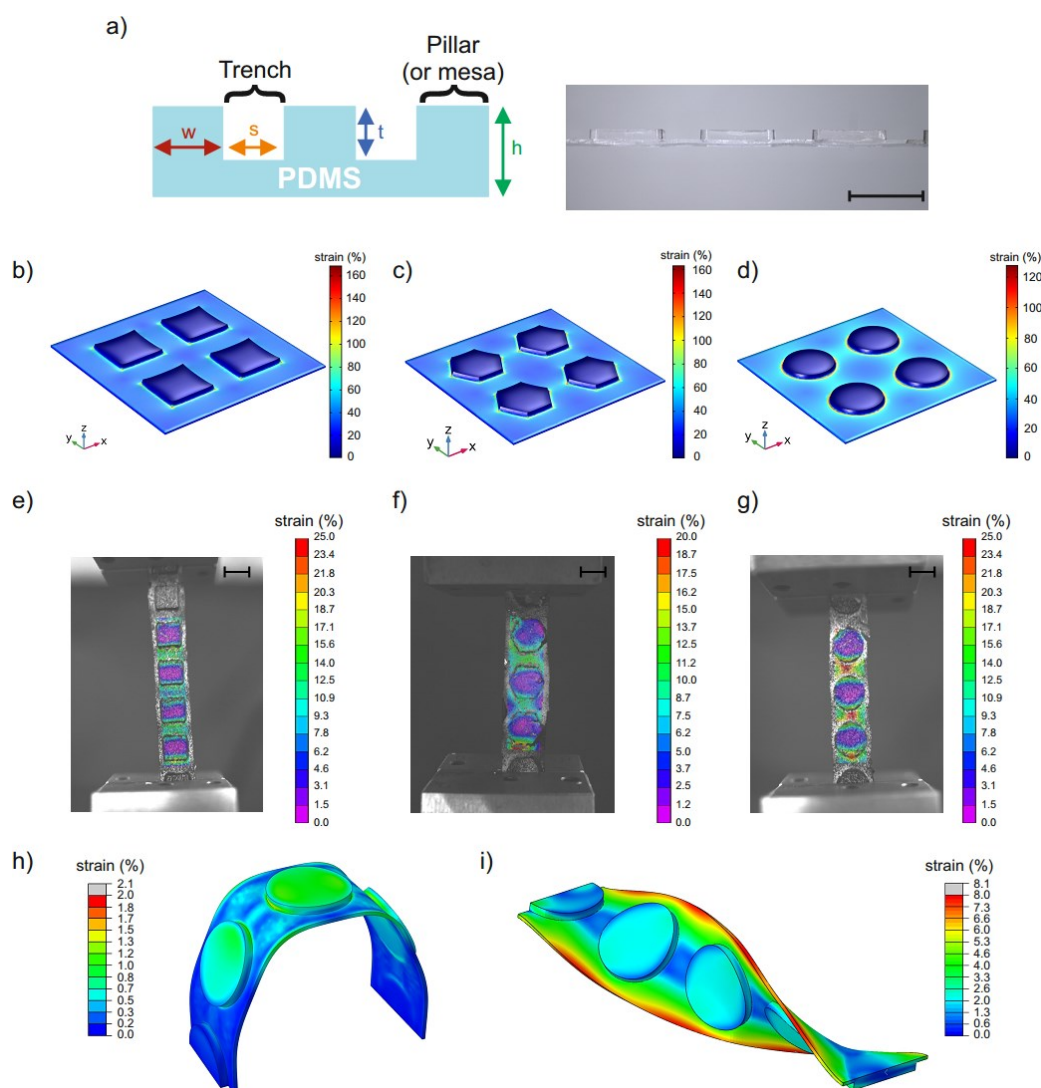
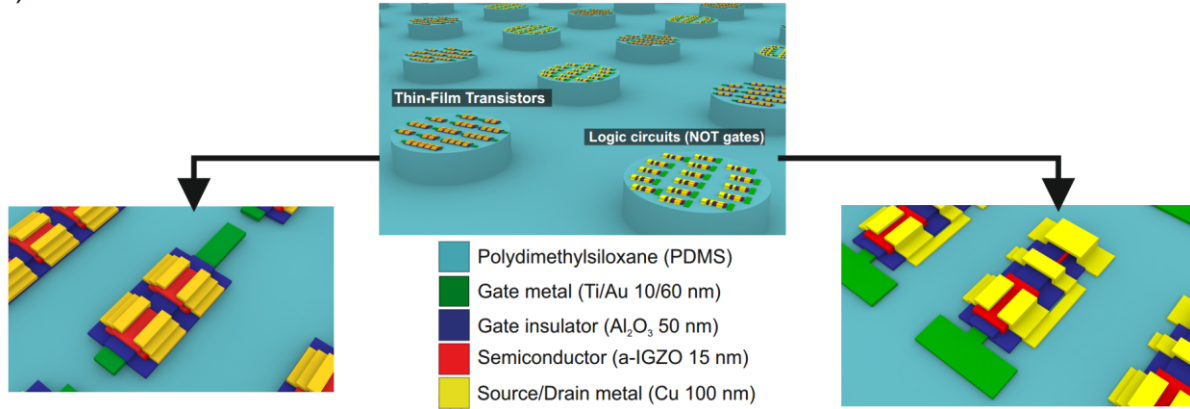
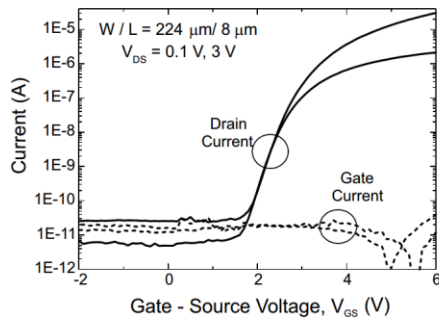


Figure 1. Engineered substrate geometry and simulations. a) To minimize the mechanical strain on top of the pillars, different geometrical parameters are analyzed: w (pillars' width), s (pillar-to-pillar distance), t (pillars' height) and h (substrate thickness). The final substrate is characterized by: $w = 5$ mm, $s = 2.5$ mm, $h = 800$ μm and $t = 560$ μm ($=0.7h$) (Scale bar: 5 mm). Different mesa shapes are evaluated while biaxial stretching (in x-y direction), equal to 20 %, is applied. Testing squared (b), hexagonal (c) and circular (d) pillars, an improved accommodation of the strain is presented in the last case. (e-g) Digital Image Correction (DIC) maps performed on the three different shapes (Scale bar: 5 mm). Different deformations are simulated to analyze the strain distribution: h) bending down to 6 mm radius and (i) twisting at 180° .

a)



b)



c)

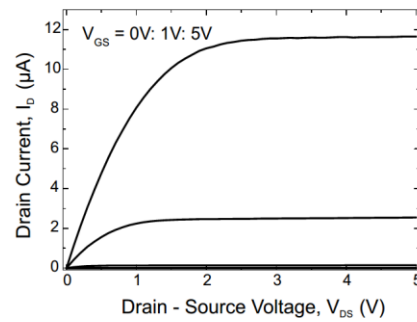


Figure 2. Schematic of the engineered flexible substrate and TFT characteristics. a) TFTs and NOT gates are directly fabricated on the pillar surface, using standard photolithographic process. The device stack is presented. (b) Transfer and (c) output characteristics of an IGZO TFT ($W/L = 224 \mu\text{m} / 8 \mu\text{m}$) on PDMS-based mesa structure.

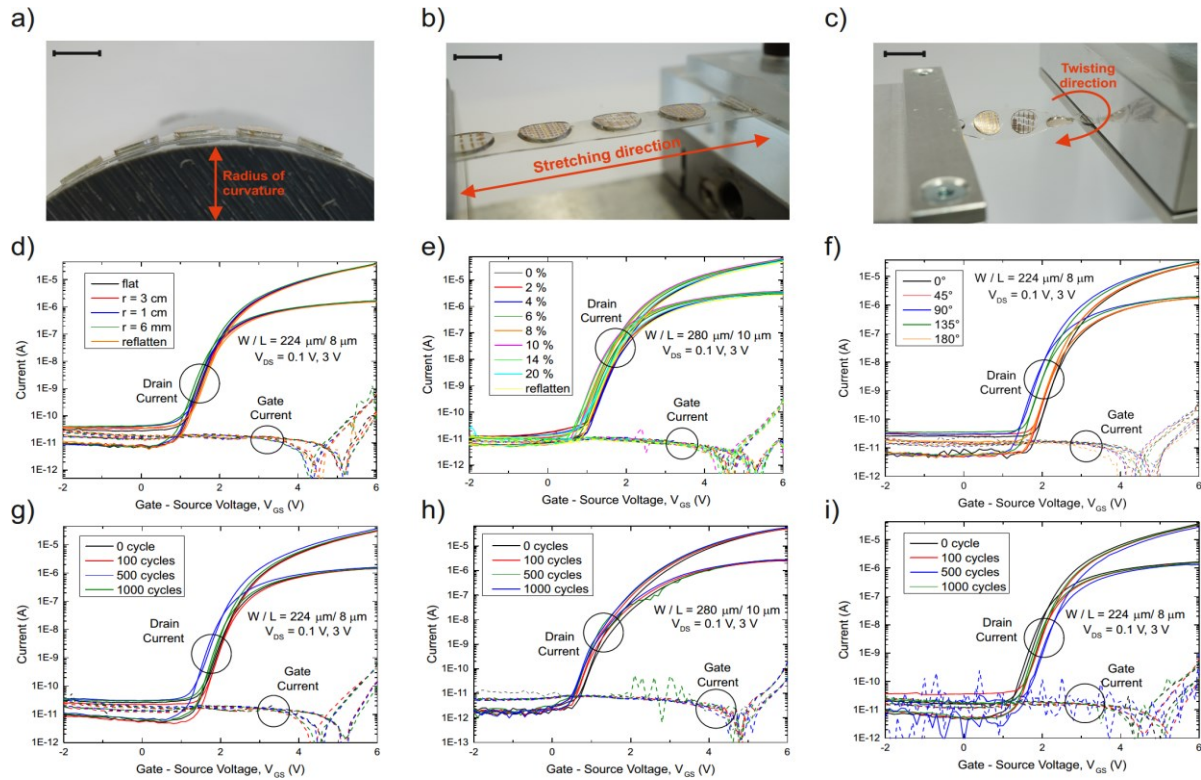


Figure 3. TFT characterization under different modes of deformation. The TFT performances are evaluated under three mechanical tests: (a) bending, (b) stretching and (c) twisting (Scale bar: 5 mm). The transfer characteristics are evaluated in static conditions: (d) bending from flat state down to 6 mm bending radius, (e) uniaxial stretching up to 20 % and (f) twisting up to 180°. The TFTs are also tested when repeatedly (g) bent to 6 mm, (h) stretched to 5 % and (i) twisted from -90° to $+90^\circ$.

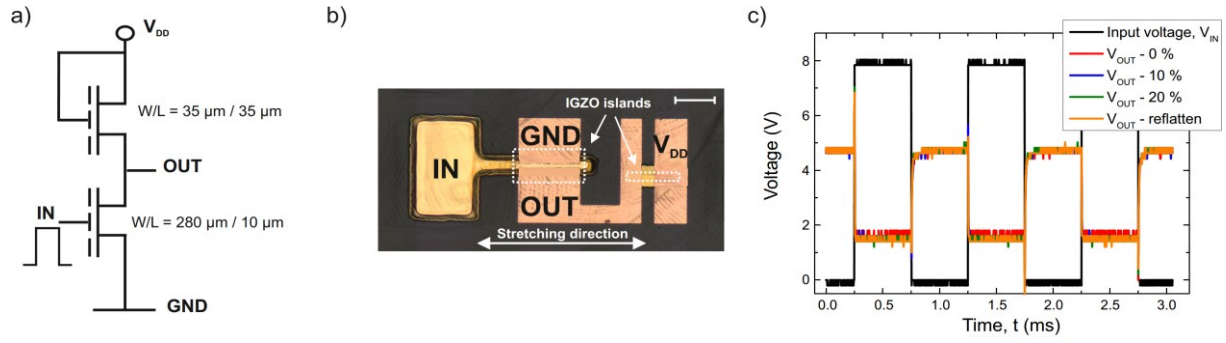


Figure 4. Inverter performance under stretching. Schematic (a), optical image (Scale bar: 200 μm) (b) and output (c) of an unipolar inverter (supply voltage $V_{DD} = 8 \text{ V}$, input voltage $V_{IN} = 0 \text{ V} - 8 \text{ V}$, input frequency $f_{in} = 1 \text{ kHz}$), stretched uniaxially up to 20 % and then re flattened. In this experiment, the stretching direction is perpendicular to the drain-source current direction.

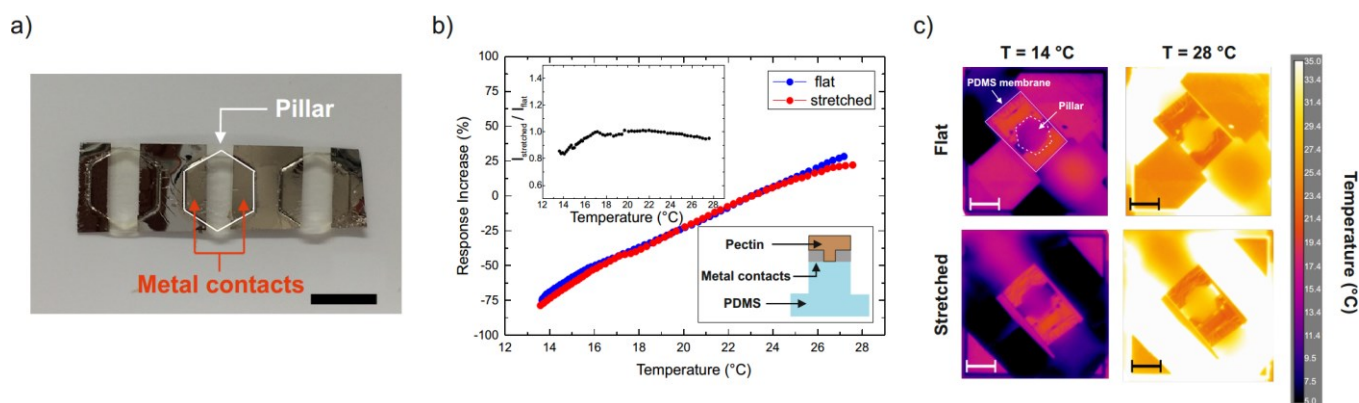


Figure 5. Pectin-based temperature sensor. (a) To highlight the sensor functionality (rather than the mechanical properties), the flexible temperature sensor is realized using hexagonal-shaped pillars, in combination with Ti/Pt metal contacts and a temperature-sensitive Pectin layer (not visible due to its high transparency) (Scale bar: 5 mm). (b) The sensor response ($\frac{Current - Current_{23^{\circ}C}}{Current_{23^{\circ}C}}$) is monitored in a temperature range from 13°C to 28°C, in flat condition and stretched at 15 %. The inset shows the ratio between the current at strain = 15 % ($I_{stretched}$) and the current at 0 % strain (I_{flat}). (c) Thermal images of a PDMS membrane, constituted by a single pillar, monitored at two different temperatures and mechanical conditions (flat and stretched at 15 %) (Scale bar: 5 mm).